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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,129	06/30/2003	Merritt Funk	071469-0304316	6686

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EXAMINER	
KOSOWSKI, ALEXANDER J	
ART UNIT	**PAPER NUMBER**
2125	

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,129	FUNK, MERRITT	
	Examiner	Art Unit	
	Alexander J Kosowski	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1) Claims 1-9, as amended 12/1/04, are presented for examination.

Claim Rejections - 35 USC § 103

2) The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3) Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reiss et al (U.S. PGPUB 2003/0014145), further in view of Fairbairn et al (U.S. Pat 6,625,497).

Referring to claim 1, Reiss teaches a method of operating a semiconductor processing system comprising determining a first state for a wafer and determining a second state for the wafer (Paragraph 033, whereby measurements may be obtained both before and after processing of the wafers to determine a first and second state); determining a process recipe to change the state of the wafer from the first state to the second state (Paragraph 0033), performing the process recipe on the wafer (Paragraph 0036), wherein the state of the wafer changes from the first state to a processed state (Paragraph 0037), determining when the processed state is not the second state (Paragraph 0033, whereby measurements may be obtained during processing), and updating the process recipe (Paragraph 0037). However, Reiss does not explicitly teach that the first and second states are determined via optical digital profiling.

Fairbairn teaches a method of operating a semiconductor processing system whereby optical digital profiling is used to measure critical dimensions of semiconductors, the results of which are used as feedback for process recipes (col. 11 lines 19-63).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to determine first and second states via optical digital profiling in the invention taught by Reiss since an optical inspection tool could be used to obtain an inspection waveform to determine if measured parameters deviate from design dimensions (Fairbairn, col. 4 lines 55-64), and since this would allow cost-effective, fast and meaningful identification and correction of CD variation without significantly reducing production throughput or yield (Fairbairn, col. 3 lines 15-18).

Referring to claim 2, Reiss teaches the method of operating a semiconductor processing system as claimed in claim 1, wherein the determining of the first state further comprises measuring at least one of an electrical property and a physical property (Paragraph 0035).

Referring to claim 3, Reiss teaches the method of operating a semiconductor processing system as claimed in claim 1, wherein the determining of the first state further comprises receiving at least one of electrical data and physical data (Paragraph 0035).

Referring to claim 4, Reiss teaches the method of operating a semiconductor processing system as claimed in claim 1, wherein the determining of the second state further comprises measuring at least one of an electrical property and a physical property (Paragraph 0035).

Referring to claim 5, Reiss teaches the method of operating a semiconductor processing system as claimed in claim 1, wherein the determining of the second state for a wafer further comprises receiving at least one of electrical data and physical data (Paragraph 0035).

Referring to claim 6, Reiss teaches the method of operating a semiconductor processing system as claimed in claim 1, wherein the determining of the process recipe comprises feeding

forward at least one process recipe based on the first and second state of the wafer (Paragraph 0030).

Referring to claim 7, Reiss teaches the method of operating a semiconductor processing system as claimed in claim 1, wherein the determining of the process recipe comprises predicting the second state using the first state of the wafer and a process model based on the process conditions (Paragraph 0047).

Referring to claim 8, Reiss teaches the method of operating a semiconductor processing system as claimed in claim 1, further comprising: determining differences between the processed state and the second state, and feeding back the differences (Paragraph 0030, whereby wafers are measured during processing).

Referring to claim 9, Reiss teaches a method of operating a semiconductor processing system comprising determining a first state for a wafer and determining a second state for the wafer (Paragraph 033, whereby measurements may be obtained both before and after processing of the wafers to determine a first and second state); determining a predicted state for the wafer, wherein a predicted process recipe is used to change the state of the wafer from the first state to the predicted state (Paragraph 0048), determining a modeled state for the wafer, wherein a process model is used to change the state of the wafer from the first state to the modeled state (Paragraph 0047), determining a measured state for the wafer (Paragraph 0033), and determining a recipe for changing the wafer state to the second state using the first state, the predicted state, the modeled state, and the measured state (Paragraphs 0037 and 0049). However, Reiss does not explicitly teach that the first and second states are determined via optical digital profiling.

Fairbairn teaches a method of operating a semiconductor processing system whereby optical digital profiling is used to measure critical dimensions of semiconductors, the results of which are used as feedback for process recipes (col. 11 lines 19-63).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to determine first and second states via optical digital profiling in the invention taught by Reiss since an optical inspection tool could be used to obtain an inspection waveform to determine if measured parameters deviate from design dimensions (Fairbairn, col. 4 lines 55-64), and since this would allow cost-effective, fast and meaningful identification and correction of CD variation without significantly reducing production throughput or yield (Fairbairn, col. 3 lines 15-18).

Conclusion

4) Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5) Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander J Kosowski whose telephone number is 571-272-3744. The examiner can normally be reached on Monday through Friday, alternating Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. In addition, the examiner's RightFAX number is 571-273-3744.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Alexander J. Kosowski
Patent Examiner
Art Unit 2125

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100